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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/757,798	01/09/2001	Jerry Thomas Bolton JR.	49581-P023US-09906909	7350

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EXAMINER	
TSE, YOUNG TOI	

ART UNIT	PAPER NUMBER
2634	10

DATE MAILED: 04/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/757,798	BOLTON, JERRY THOMAS	
	Examiner	Art Unit	
	YOUNG T. TSE	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 January 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4,6,9*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed 11 February 2001 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered. References G, H, and I have not been considered by the examiner. Further, reference F "Complex Signals: Part I" includes pages 27-33 only, published in 1989. However, pages 57 to 115 (some of the pages are missing) are covered in F "Complex Signals: Parts II-IV", published in 1990. Applicant is requested to make the changes in the PTO-1449 if Parts II-IV to be included in the IDS.

Drawings

2. Figure 9 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to because an arrow flow is not labeled in Figure 12 between elements 122 and 1023 (top portion). A proposed drawing correction or

corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: the reference signs "5" and "5'" are not labeled in Figure 5 as mentioned on page 8, lines 6 and 23 of the specification; the reference sign "842" is not labeled in Figure 8 as mentioned on page 19, line 10 of the specification; the reference signs "1204" and "1205" are not labeled in Figure 12 as mentioned on page 16, lines 12-13 of the specification; and the reference signs "210", "211", "MASH A", and "MASH B" are not shown in any the Figures as mentioned on page 21, lines 21-23. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: the reference sign "120" labeled in Figure 12 is not mentioned in the specification. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

6. Claims 2, 14-19 and 22 are objected to because of the following informalities: in claim 2, line 2, the phrase "an output of said set of differentiators" appears to read -- an output of each of said set of differentiators – for accuracy; wherein claim 14 depends upon claim 2; in claim 15, line 2, "an input" should be – an input signal --; in claim 16, lines 3 and 5, "reversed input" should be – inversed input signal – and line 6, "said quantized signal" should be – quantized signal as said first modulated signal – for clarity; in claim 17, line 2 and 5, "signal" and "said subsequence modulated signal" should be – signals – and – a subsequence modulated signal --, respectively; wherein claim 18 depends upon claim 17; in claim 19, lines 2-3, the phrase "said producing said first intermediate modulating signal step" should be -- said step of producing said first intermediate modulating signal --; and in claim 22, lines 2-3, the phrase "said producing said first intermediate modulating signal step" should be -- said means for producing said first intermediate modulating signal – since claim 20 is an apparatus claim. Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 1-23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which

was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The configuration of claims 1, 10, 15, and 20 does not correspond to the disclosure of the drawings. For example, claim 1 recites a set of differentiators disposed in each of said at least one consequence stage, however, as shown in Figure 8, the second stage includes one differentiator only; claim 10 recites the first delta-sigma modulator comprises a multi-stage delta-sigma modulator, however, as shown in Figure 8, the first delta-sigma modulator comprises a one-sate delta-sigma modulator only; claim 15 recites a step of programming at least one of said subsequences to be different from said first reference, according to the present invention discussed in the specification and shown in the Figures, it appears no circuitry is shown for programming references 6120, 7130, and 8140 as shown in Figure 8; and claim 20 recites means for providing said modulated output signal to an output of said multi-order delta-sigma modulator, however, it appears no additional circuitry is shown other than the summing circuit 600 of Figure 8 for providing said modulated output signal to an output of said multi-order delta-sigma modulator; wherein the dependent claims 2-9, 11-14, 16-19, and 21-23 are depended upon claims 1, 15, and 20.

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 4 and 13-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 4, the claim subject matter is unclear that what are the number of digital differentiators to be used in the set of differentiators in each of the subsequence stages.

Claims 13 and 14 recite the invention constructed substantially on a single integrated circuit substrate. However, claim 1 recites a multi-staged delta-sigma modulator comprising a plurality of stages, in other words, it is unclear the multi-staged delta-sigma modulator or each of the stages is constructed substantially on a single integrated circuit substrate. According to the present invention, in claim 13, line 1, the phrase "The invention of claim 1" should be – The modulator of claim 1 wherein said multi-staged delta-sigma modulator is – and claim 14 should be cancelled.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. Claims 1-2, 13-18 and 20-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Adach et al.

Adachi et al. (US Patent No. 6,717,998 B2) discloses a fraction part control circuit or multi-stage or multi-order delta-sigma modulator 5e in Figure 14.

The fraction part control circuit 5e comprises a first delta-sigma stage, a second delta-sigma stage, and a summation circuit 240 for summing the modulated signal of the first delta-sigma stage and the second delta-sigma stage to produce a multi-order modulated signal. The first delta-sigma stage includes a second-order delta-sigma modulator circuit 200 having adder 208, integrator 201, quantizer 202, feedback circuit 203, and multiplier 207; a delay 209; a multiplier 211; and a subtractor 210. The second delta-sigma stage includes a second-order delta-sigma modulator circuit 220 having adder 228, integrator 221, quantizer 222, feedback circuit 223, and multiplier 277; and a second-order differential circuit 230. See col. 21, line 29 to col. 22, line 23.

With respect to claims 1, 15 and 20, the first delta-sigma stage correspond to the first delta-sigma modulator of a first stage having a quantization error Q1 or first reference signal to be added by the quantizer 202, the second delta-sigma stage corresponds to the at least one subsequence delta-sigma modulator of at least one subsequence stage cascade from the first stage having a quantization error Q2 or a reference signal variable in relation to the a quantization error Q1, and the second-order differential circuit 230 corresponds to the set of differentiators coupled to the output of the quantizer 222. See col. 22, lines 24-28.

With respect to claim 2, the summation circuit 240 for adding the output of the first delta-sigma stage and the output of the second-order differential circuit 230.

With respect to claims 13 and 14, the first delta-sigma stage, the second delta-sigma stage, the second-order differential circuit 230, and the summation circuit 240 are integrated in the fraction part control circuit 5e or substrate.

With respect to claim 16, the claimed subject matter is clearly shown in the first delta-sigma stage of the fraction part control circuit 5e.

With respect to claims 17 and 18, the claimed subject matter is clearly shown in the second delta-sigma stage of the fraction part control circuit 5e.

With respect to claim 21, the second-order differential circuit 230 is used for differentiating the subsequence intermediate modulated signals.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 3, 12, 19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adach et al. in view of Duffy et al.

Although Adach et al. does not explicitly show or suggest the input signal of the fraction part control circuit 5e is a digital signal (claim 3) and provides an interpolation filter prior the fraction part control circuit 5e for increasing a sampling rate of the input signal (claims 12, 19 and 22),

Puffy et al (US Patent No. 5,196,850) discloses a digital-to-analog converter modulator in Figure 1 which includes a digital delta-sigma modulator 16 for modulating a digital signal 14 through an interpolation filter 12 for increasing a sampling rate of the digital signal 14 before processing the sampled digital signal to the digital delta-sigma modulator 16.

Applicant note, it is well known to a person skill in the art that a delta-sigma modulator is either an analog-to-digital converter for converting an analog signal into a digital signal or a digital-to-analog converter for converting a digital signal into an analog signal, it depends on the requirements of the circuitry a digital converter or an analog converter is needed.

Therefore, it is obvious to one of ordinary skill in the art to use a digital signal or an interpolation filter for increasing the sampling rate of the digital signal before processing the digital input signal in Adach's fraction part control circuit 5e as taught by Puffy when the fraction part control circuit 5e is operated in digital conversion in order to convert a digital input signal of a digital-to-analog delta-sigma modulator into an analog signal to an analog circuit.

15. Claims 5-9, 11 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adach et al in view of the prior art Figure 5 of the instant application.

Although Adach shows a total two stages in the fraction part control circuit 5e only, but not more than two stages as recited in claims 5 and 11, wherein only one differential circuit 230 shown in one of the two stages. It is well known in the delta-sigma modulator art that higher order of delta-signal modulator is commonly used, for

example, the multi-order delta-sigma modulator shown in the prior art Figure 5 of the instant application includes four stages, the second to the forth stages each comprises a set of differential circuit.

Therefore, it would have been obvious to one of ordinary skill in the art to include more stages in Adach's fraction part control circuit 5e in order to reduce the among of correlation between the input and the quantization noise.

With respect to claims 6-9 and 23, although the quantization errors or reference signals Q1 and Q2 shown in Adach's fraction part control circuit 5e are different from each other as recited in claim 6 (col. 23, lines 1-17). However, it is the choice of design to determine what values to be used in the quantization errors of the quantizers as recited in claims 7-9 and 23 depended upon the requirements of the other circuits.

16. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Adach et al in view of Puffy et al. as applied to claim 3 above, and further in view of prior art Figure 5 of the instant application.

As discussed in paragraph 15 above that although Adach shows a total two stages in the fraction part control circuit 5e only, but not more than two stages as recited in claim 4, wherein only one differential circuit 230 shown in one of the two stages. It is well known in the delta-sigma modulator art that higher order of delta-signal modulator is commonly used, for example, the multi-order delta-sigma modulator shown in the prior art Figure 5 of the instant application includes four stages, the second to the forth stages each comprises a set of differential circuit.

Therefore, it would have been obvious to one of ordinary skill in the art to include more stages in Adach's fraction part control circuit 5e in order to reduce the among of correlation between the input and the quantization noise.

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

References Endo et al., Cabler, Harris et al., Mitama, Okuda et al., and Sridharan are made of record as describing a related multi-stage or multi-order delta-signal modulator having a plurality of stages.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Young Tse** whose telephone number is **(703) 305-4736**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Stephen Chin**, can be reached at **(703) 305-4714**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

P.O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

(703) 872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal

Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Young T. Tse
Primary Examiner
4/17/04